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U.S. UTILITY Patent Application

APPL NUM 10091934	FILING DATE 03/06/2002	CLASS 716	SUBCLASS 1	GAU 2825	EXAMINER <i>Levin</i>
**APPLICANTS: Alon Amir; Goren David; Gordin Rachel; Livshitz Betty; Sherman Anatoly; Zelikson Michael;					
**CONTINUING DATA VERIFIED:					
** FOREIGN APPLICATIONS VERIFIED:					
PG-PUB <input type="checkbox"/> DO NOT PUBLISH <input type="checkbox"/> RESCIND <input type="checkbox"/>					
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no 35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no Verified and Acknowledged Examiners's initials				ATTORNEY DOCKET NO IL920020007US1	
TITLE : Interconnect-aware methodology for integrated circuit design					

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NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for: O.G.
ISSUE FEE		Primary Examiner	DRAWING	
Amount Due	Date Paid		Sheets Drwg.	Figs.Drwg.
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE	Application Examiner	
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